DIALOG(R)File 351:Derwent WPI

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Firmware mechanism for correcting soft errors e.g. for microprocessors, includes processor having dual execution cores and a non-volatile memory that stores an error recovery routine
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Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200146806	A1	20010628	WO 2000US41079	A	20001004	200167 B
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Priority Applications (No Type Date): US 99469963 A 19991221; US 2000608824 A 20000630; US 2003622910 A 20030718; US 2003623396 A 20030718
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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AU 200116318	A	G06F-011/16	Based on patent WO 200146806
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US 6625749	B1	G06F-011/00	
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			Cont of application US 2000608824
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Cont of patent US 6631338
GB 2373900 B G06F-011/16 Based on patent WO 200146806
US 6947859 B2 H03K-019/003 Cont of application US 2000752258
Cont of patent US 6631338

Abstract (Basic): WO 200146806 A1

NOVELTY - Computer system includes processor having dual execution cores and a non-volatile memory that stores an error recovery routine. The processor's execution cores operate in lock step when the processor is in a redundant execution mode, and they operate independently when the processor is in a split execution mode. The error recovery routine is invoked when the processor detects a soft error while operating in the redundant execution mode.

DETAILED DESCRIPTION - The error recovery routine switches the processor to split execution mode. In split mode. each execution core saves uncorrupted processor state data to a designated memory location and updates any corrupted data with corresponding processor state data from the other execution core. The error recovery routine returns the processor to redundant mode, initializes each execution core with the recovered processor state data and returns control of the processor to the program thread that was executing when the soft error was detected.

INDEPENDENT CLAIMS are also included for the following:

(a) method of handling soft errors;

(b) machine readable medium

USE - For microprocessors.

ADVANTAGE - Firmware-based mechanism corrects soft errors in a dual core processor that can be switched between redundant execution mode and split execution mode.

DESCRIPTION OF DRAWING(S) - The flow chart shows the method for recovering from soft errors.

pp; 39 DwgNo 3/7

Title Terms: FIRMWARE; MECHANISM; CORRECT; SOFT; ERROR; MICROPROCESSOR; PROCESSOR; DUAL; EXECUTE; CORE; NON; VOLATILE; MEMORY; STORAGE; ERROR; RECOVER; ROUTINE
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